Short-Channel Double-Gate FETs with Atomically Precise Graphene Nanoribbons

Z. Mutlu[1†], Y. Lin[1†], G. B. Barin[2†], Z. Zhang[3], G. Pitner[4], S. Wang[2], R. Darawish[2], M. Di Giovannantonio[2], H. Wang[4], J. Cai[5], M. Passlack[4], C. H. Diaz[4], A. Narita[6], K. Müllen[6], F. R. Fischer[1], P. Bandaru[3], A. C. Kummel[3], P. Ruffieux[2], R. Fasel[2], and J. Bokor[1]

[1]University of California, Berkeley, Berkeley, CA, USA. Email: zmutlu@berkeley.edu

[2]Empa, Swiss Federal Laboratories for Materials Science and Technology, Dübendorf, Switzerland.

[3]University of California, San Diego, San Diego, CA, USA.

[4]Corporate Research, Taiwan Semiconductor Manufacturing Company, San Jose, CA, USA.

[5]Corporate Research, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan.

[6]The Max Planck Institute for Polymer Research, Mainz, Germany. †These authors contributed equally.

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***Abstract*—**High performance graphene nanoribbon (GNR) transistors require seamless integration of GNRs with high-k dielectrics, which remains unexplored. This work evaluates performance of bottom-up synthesized 9-atom armchair GNRs (9-AGNRs) in short channel back-gate (BG) and double-gate (DG) FETs. Top-gate (TG) dielectric bilayers consisting of 1–1.25 nm Al_2O_3 and 2.5 nm HfO_2 are deposited on 9-AGNRFETs with a 5.5 nm HfO_2 BG dielectric. Devices exhibit excellent I_{ON}/I_{OFF} up to ~10^5 and I_{ON} up to ~60 µA/µm (~2.4 µA per GNR). DG enables improved subthreshold swing (*SS*) and low hysteresis owing to its superior electrostatic control. We also identify and quantify through numerical simulations the improvements in materials and process that would enable GNRs with performance close to outstanding theoretically predicted metrics.

I. INTRODUCTION

Bottom-up chemically synthesized GNRs present an attractive alternative to CNTs as channel material for future transistor technologies. Due to their deterministic growth process[1], such GNRs possess identical electronic properties[2] en masse and, unlike top-down GNRs, lack edge defects that reduce mobility and degrade carrier transport. GNRFETs have been demonstrated[3,4], but several challenges[5] remain, such as short ribbon length, high *SS*, hysteresis, and Schottky barrier (SB) contacts. TG high-k dielectric improves electrostatic control in short-channel CNTFETs[6]. GNRs having similar properties should also benefit from TG, which is unexplored. Here, we evaluate the performance of 9-AGNRs as transistor channel. Transistor structures fabricated include BG, TG and DG FETs. DG offers superior electrostatic control enabling improved *SS* and low hysteresis. Challenges, and opportunities of GNRs as transistor channel are discussed, together with possible further improvements, for potential high-performance logic applications.

II. GNR GROWTH AND DEVICE FABRICATION

9-AGNRs were grown on Au(111)/mica from 3′,6′-diiodo-1,1′:2′,1″-terphenyl (DITP) via a surface-synthetic protocol[7] (Fig. 1a). STM imaging (Fig. 1b) shows that the GNRs are straight and densely packed and have an average length of ~48 nm (Fig. 1d). Theoretically predicted bandgap of the free-standing and the substrate-supported 9-AGNR is 2.29 eV, and 1.4 eV, respectively[8]. The GNR width is 0.95 nm. The GNRs synthesized from the iodine (I) precursor in this study are >3 times longer than those obtained from the bromine (Br) precursor[9]. Non-contact AFM image (Fig. 1c) confirms planar 9-AGNR growth, proving edge carbon atoms are passivated by single hydrogen atoms[9]. The strong characteristic radial breathing-like mode (RBLM) and C-H, D and G modes in the Raman spectra (Fig. 2a) confirms that the GNRs are uniform and passivated with hydrogens[10]. The GNRs are wet transferred onto a pre-patterned SiO_2/Si chip containing local BG devices with W gate metal capped with 5.5 nm HfO_2 ALD[10]. AFM images (Fig. 2d, e) indicate that the transferred GNR film is smooth (<0.6 nm) and uniform [10]. The well-preserved fingerprint Raman peaks (Fig. 2b) suggest that the ribbons remain intact[10]. BG GNRFETs (Fig. 3a) with Pd contacts, 20-65 nm channel length (L) and 30–200 nm channel width (W) (Fig. 3b, c), were fabricated[11]. For DG GNRFET (Fig. 3b) fabrication, 1–1.25 nm Al_2O_3 (referred here as "nanofog") was deposited as a conformal seeding layer at 50 °C using TMA and H_2O directly atop BG devices[14], followed by 2.5 nm HfO_2 ALD using TDMAH and H_2O at 200 °C. AFM image (Fig. 2f) show an atomically smooth (<0.5 nm) pinhole-free surface, indicating uniform HfO_2 growth. The well-preserved GNR Raman features and the absence of the C-O and O-H peaks suggest that the GNRs are not damaged[10] and nor chemically altered[15] (Fig. 2c). Pd TG metal was then deposited.

III. SHORT-CHANNEL GNRFETS

The drain current (I_D)–gate voltage (V_{GS}) plot of a representative BG GNRFET (Fig. 4a) shows a p-type behavior, with an on-state current (I_{ON}) of ~1 µA at a drain voltage (V_{DS}) of −1 V, and an on-off current ratio (I_{ON}/I_{OFF}) of ~10^5. The statistical distribution of the I_{ON} (Fig. 5a) and I_{ON}/I_{OFF} (Fig. 5b) in 274 devices shows a I_{ON}/I_{OFF} up to 10^5, and a I_{ON} up to ~60 µA/µm (~2.4 µA per GNR), the highest reported for bottom-up synthesized GNRs[3,4,11,12]. I_{ON} and I_{ON}/I_{OFF} variations are likely due to variations in contact length (L_C) of the GNR-Pd interface, in the number of GNRs bridging the channel, and in the electrode edge roughness[13]. Device yield, defined as the percentage of devices with their

I_D >10 times larger than their gate leakage current (I_G), is almost 100%, much higher than that of the FETs with the GNRs grown from the Br precursor[4]. The improvements in the I_{ON} and yield in this work can be explained by the larger number of GNRs bridging the channel and longer L_C. Nevertheless, super-linear I_D–V_{DS} curves (Fig. 4b) indicate a SB-limited performance. DG 9-AGNRs are characterized using BG sweep (at fixed TG bias), TG sweep (at fixed BG bias), and DG sweep (BG and TG are swept simultaneously). Fig. 6a, b display the statistical distribution of the I_{ON} and I_{ON}/I_{OFF}, respectively, in 113 devices in BG, TG and DG sweeps. DG sweep shows the highest I_{ON} and I_{ON}/I_{OFF} due to better electrostatic control. Fig. 7c shows the maximum I_G from 113 devices before and after TG fabrication. BG I_G is reduced after TG fabrication, possibly due to the healing of BG dielectric during TG dielectric deposition. While TG I_G is slightly higher than BG I_G possibly because of the thinner TG dielectric thickness, it is still comparable to the reported values for the BG GNRFETs[4]. Fig. 7a plots the I_D–V_{GS} of a representative 9-AGNR device before and after TG fabrication. TG fabrication results in elimination of hysteresis, indicating good TG dielectric/GNR interfaces and passivation effect from the charge trapping by air molecules[16]. Fig. 7b shows significant improvement in the *SS* for DG FETs. 85% decrease in the *SS* indicates potential of DG for high performance GNR transistors.

IV. NUMERICAL SIMULATIONS

A semi-analytical device model is developed to capture the main experimental features of 9-AGNR transistors, including Schottky contact, short L_C, scattering, parasitic capacitances, GNR-GNR screening, and trapped charges. The model is based on the self-consistent solutions of the Landauer-Büttiker formalism and the numerically simulated electrostatics. Fig. 8 shows a typical device band diagram. The model is first used to fit the measured device characteristics (Fig. 9), from which device parameters can be extracted as summarized in Fig. 9c. The SB height (Φ_B) is around 0.4 eV. With 1.5-nm-EOT local BG, the scaling length λ is 1.8 nm, which determines both gate coupling efficiency and SB width. Although device performance is still limited by the transport at the SB, such a thin barrier gives rise to substantial tunneling current, which enhances the I_{ON} as compared to thicker gate dielectric devices[4]. The numerically simulated electrostatics of BG and DG GNR transistors (Fig. 10a, b) suggest that electrostatic control is more efficient for DG, while λ for the BG and DG are extracted to be similar, which explains the comparable I_{ON} measured on BG and DG devices. To account for the improvement of the *SS* for DG devices, we also simulated the bundled GNR cases in which effective GNR layer thickness is several times larger. DG structure with bundled GNRs has a similar gate coupling efficiency as compared to the single-GNR case, whereas the gate coupling efficiency for BG with bundled GNRs is much worse (Fig. 10c), which agrees with the observed *SS* differences for DG and BG devices. Our analysis suggests that GNR bundling needs to be reduced to further improve the *SS*.

Starting from the fitting, the key device parameters are then varied to project device performance. The major trends are summarized as following: 1) The I_{ON} can be enhanced by several times if both Φ_B and λ are reduced, while several hundred milli-eV of Φ_B only slightly degrades the I_{ON} if the gate stacks are fully optimized, and λ is < 2 nm (Fig. 11). The I_{ON} enhancement is 0.09% and 0.17% per meV of Φ_B reduction when λ is 2 nm and 5 nm, respectively. 2) The contact-limited device performance is more likely to be caused by short L_C (Fig. 12a), or equivalently, short ribbon lengths (Fig. 12b). To address this issue, the synthesis needs to be improved to increase the ribbon length. 3) The effect of the defects in the GNR (as indicated by the mean free path, l_{MFP}) is less critical (Fig. 12c) in the current device structure, although a previous study[17] suggested that the "bite" defects may become the major bottleneck of the device performance once the contact resistance is much improved. Elimination of AGNR defects is a challenge for the synthesis process. 4) There is a strong correlation between gate coupling efficiency (*SS*) and the spatial distributions of the GNRs. Two factors are to be considered: first, the redistributions during GNR transfer may lead to the ribbon overlap or bundling, as has been discussed earlier (Fig. 10); second, the high GNR density (~500 μm^{-1} (Fig. 1b)) introduces severe electrostatic screening between neighboring GNRs, which would degrade gate capacitances drastically (Fig. 13). The screening effect is significant for both BG and DG. The regular and aligned placement of GNRs is a subject of future research.

Fig. 14 displays the benchmark. Although further improvements are needed to realize GNR FET metrics close to the projected values, the demonstration of short-channel GNR FETs with highest on-state current, excellent switching performance, and uniform high-k dielectric growth on relatively inert ultranarrow GNR surface offering superior electrostatic control is an important step towards high performance GNR transistors.

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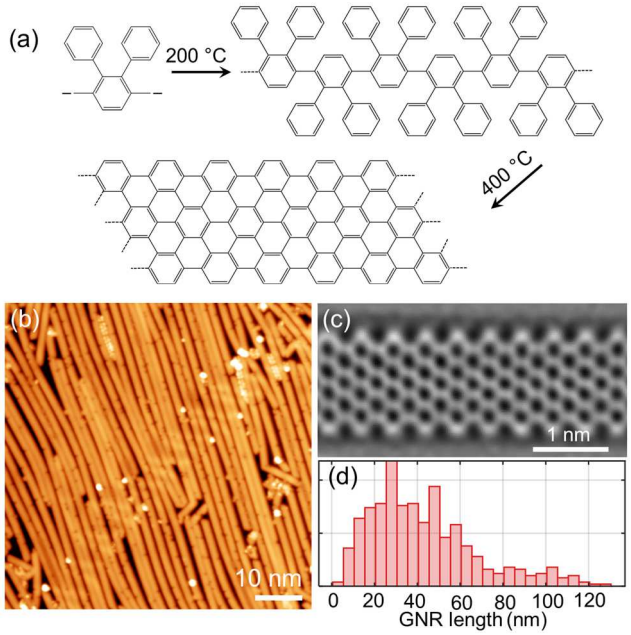


Figure 1. (a) Reaction path for the growth of 9-AGNRs on Au(111) substrate. STM (b), non-contact AFM (c) images, and the length distribution (d) of 9-AGNRs.

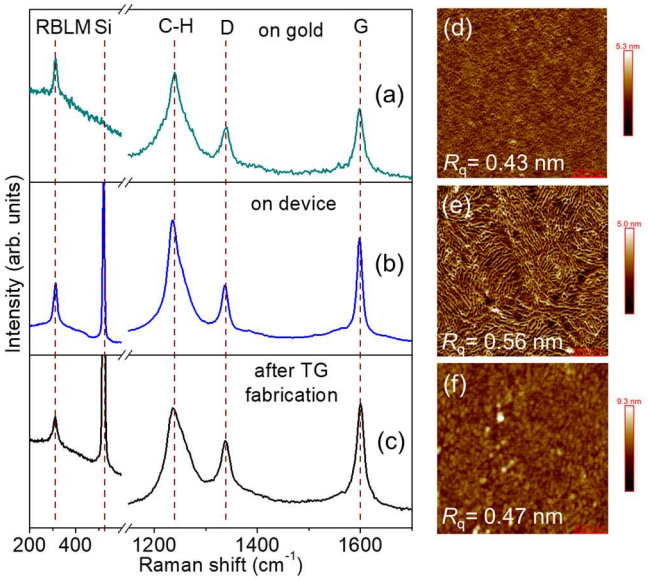


Figure 2. Raman spectra of the GNRs on gold (a), after transfer and device processing (b), and after TG dielectric deposition (c), collected with 785 nm wavelength laser excitation. AFM images (1×1 μm) of the local back gate (HfO_2/W/SiO_2/Si) before (d) and after (e) the GNR transfer, and after (f) TG dielectric deposition.

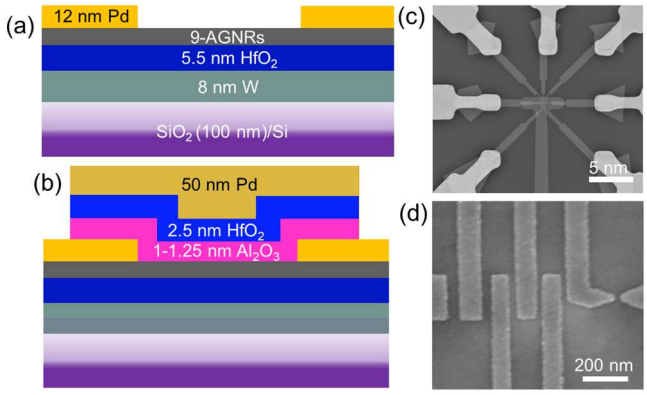


Figure 3. Cross-sectional diagrams of BG (a) and DG (b) GNRFETs. Low (c) and high (d) magnification SEM images of BG FET before TG fabrication.

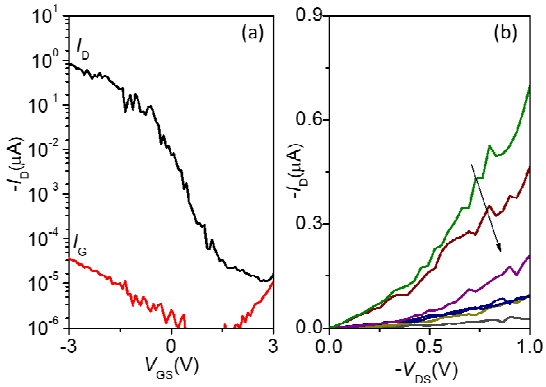


Figure 4. I_D–V_{GS} (a) and I_D–V_{DS} (with V_{GS} varying from −3 V to 3 V with 0.5 V steps) (b) characteristics of a BG GNRFET. All device measurements are performed at V_{DS}= −1 V under vacuum.

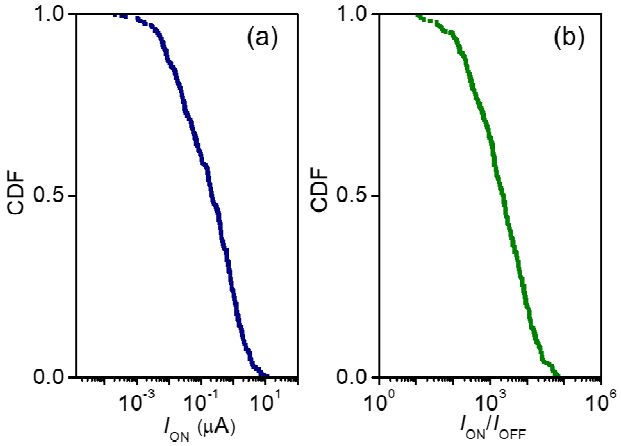


Figure 5. Cumulative distribution function (CDF) of the I_{ON} (a) and the I_{ON}/I_{OFF} (b) in 274 BG devices. The devices show an I_{ON}/I_{OFF} up to ~10^5, and an I_{ON} up to ~12 μA (2.4 μA/GNR) for a device with L= ~40 nm and W= 200 nm (~5 GNRs per the channel).

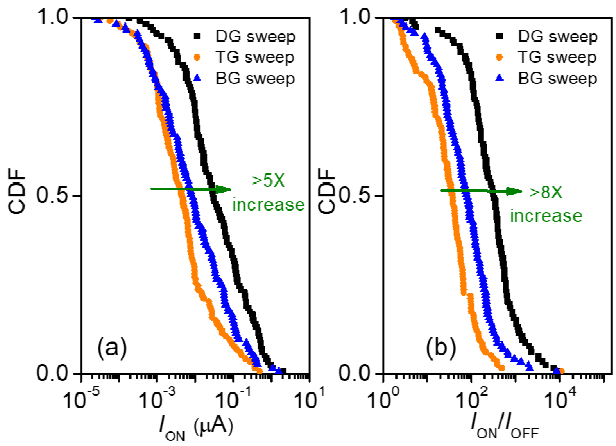


Figure 6. CDF of the I_{ON} (a) and the I_{ON}/I_{OFF} (b) in 113 DG FETs with BG (V_{BG}= 3 V to −3 V, V_{TG}= 0), TG (V_{TG}= 2 V to −2 V, V_{BG}= 0), and DG (V_{DG}=V_{BG}=V_{TG}= 2 V to −2 V) sweeps.

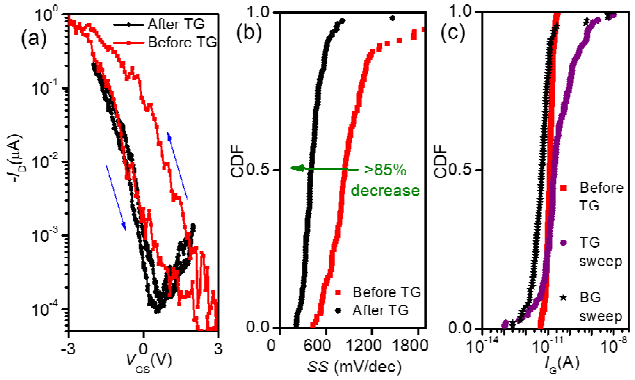


Figure 7. (a) I_D–V_{GS} characteristics of a 9-AGNR FET before and after (DG sweep) TG fabrication (b) CDF of the *SS* in 113 devices before and after (DG sweep) TG fabrication. (c) CDF of the I_G in 113 devices before TG fabrication (at V_{BG}= 2 V), and after TG fabrication wth BG (at V_{BG}= 2 V, V_{TG}= 0 V) and TG (at V_{TG}= 2 V, V_{BG}= 0 V) sweeps.

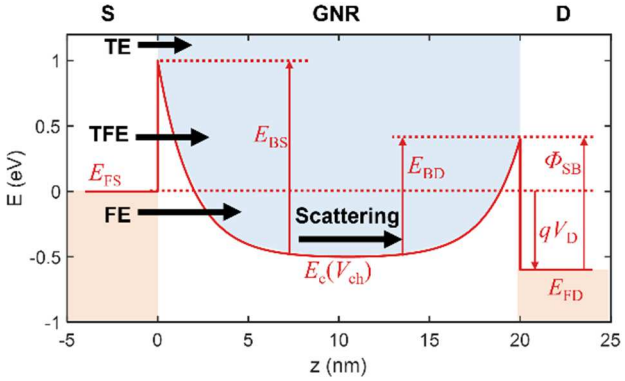
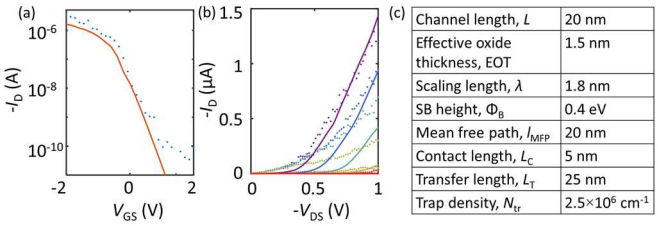


Figure 8. The energy band diagram along 9-AGNR channel. The thermionic emission (TE) current, the thermionic field emission (TFE) current, and the field emission (FE) current are considered at the SB; and the carrier scattering is considered in the GNR channel.



(c)	
Channel length, L	20 nm
Effective oxide thickness, EOT	1.5 nm
Scaling length, λ	1.8 nm
SB height, Φ_B	0.4 eV
Mean free path, l_{MFP}	20 nm
Contact length, L_C	5 nm
Transfer length, L_T	25 nm
Trap density, N_{tr}	2.5×10^6 cm^{-1}

Figure 9. Experimental verification of the single 9-AGNR FET model. (a) I_D–V_{GS} characteristics with V_{DS}= −1 V. (b) I_D–V_D characteristics with V_{GS} varying from −1.8 V to 0.7 V with 0.5 V steps. The solid lines are simulation results. The dots are experimental results. (c) Parameters used in the simulation that best matches the experimental results.

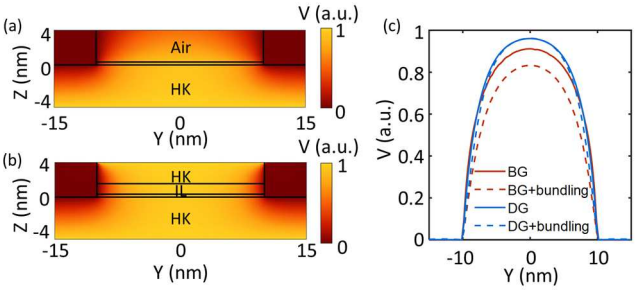


Figure 10. Numerical simulation of the electrostatics of BG and DG GNR transistors. (a) Potential mapping of the BG transistor. (b) Potential mapping of the DG transistor. (c) Potential along the GNR channel.

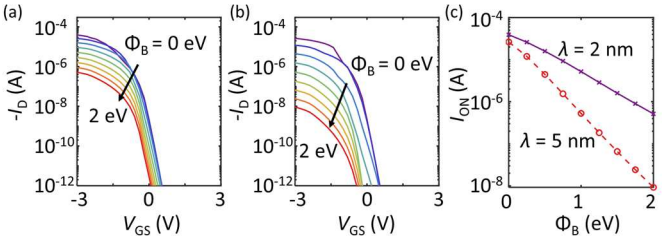


Figure 11. The effects of Φ_B and λ. (a) simulated I_D–V_{GS} characteristics with λ= 2 nm, V_{DS}= −1 V, and different Φ_B. (b) simulated I_D–V_{GS} characteristics with λ= 5 nm, V_{DS}= −1 V, and different Φ_B. (c) simulated I_{ON} versus Φ_B when λ is 2 nm (purple), and 5 nm (red).

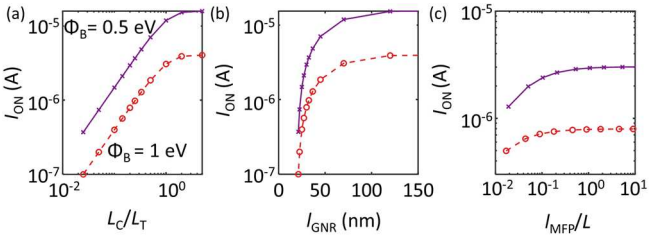


Figure 12. Short contact limited I_{ON} in single-GNR FETs. (a) Simulated I_{ON} versus L_C/L_T when Φ_B is 0. 5 eV (purple), and 1.0 eV (red). (b) Simulated I_{ON} versus I_{GNR} (c) Simulated I_{ON} versus I_{MFP}/L. V_{DS}= -1 V, V_{GS}= -3 V.

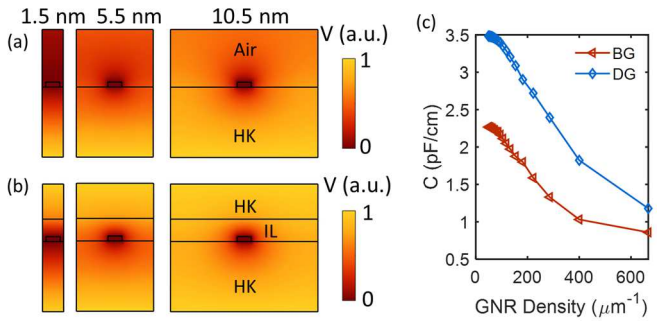


Figure 13. The effects of GNR-GNR screening. (a) Potential mapping of the BG GNR transistor with 1.5 nm, 5.5 nm, and 10.5 nm GNR-GNR spacing. (b) Potential mapping of the DG GNR transistor with 1.5 nm, 5.5 nm and 10.5 nm GNR-GNR spacing. (c) Extracted capacitance per GNR as a function of GNR density for BG and DG structures.

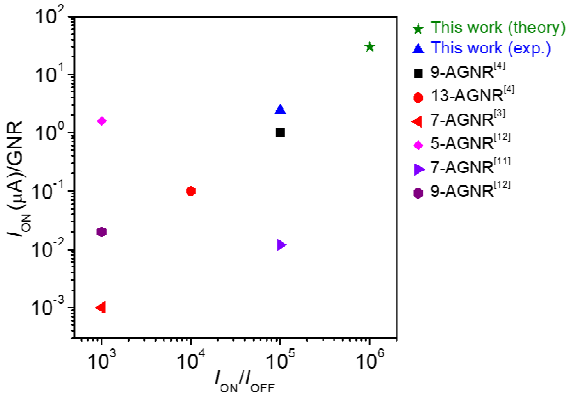


Figure 14. GNR FET devices benchmark. The maximum I_{ON} (per GNR) and I_{ON}/I_{OFF} ratio values are obtained from the devices fabricated with bottom-up synthesized 5-, 7-, 9- and 13-AGNRs at $|V_{DS}|$= 1 V.